REMARKS/ARGUMENTS

Claims 20-24 and 26-30 were pending in this application. Claims 14-19 have been withdrawn. Claim 20 has been amended. Claim 21 has been cancelled. No claims have been added. Hence, claims 20, 22-24 and 26-30 are pending after entry of the amendments presented herein. Reconsideration of the subject application as amended is respectfully requested.

Claims 20 and 21 stand rejected under 35 U.S.C. § 102(e) as being anticipated by the cited portions of U.S. Patent No. 5,391,904 to Asami *et al.* (hereinafter "Asami").

Claim 20 stands rejected under 35 U.S.C. § 102(e) as being anticipated by the cited portions of U.S. Patent No. 5,342,7944 to Wei *et al.* (hereinafter "Wei").

Claims 22-23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wei, in view of the cited portions of U.S. Patent No. 5,286,518 to Cain *et al.* (hereinafter "Cain").

Claims 24 and 26-28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wei in view of the cited portions of U.S. Patent No. 3,808,475 to Buelow *et al.* (hereinafter "Buelow").

Claims 29-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Wei, in view of Buelow, and further in view of the cited portions of U.S. Patent No. 5,313,079 to Brasen *et al.* (hereinafter "Brasen").

In the Advisory Action, the drawing corrections filed on December 1, 2004, were accepted.

Claim 20 has been amended herein to include subject matter from claim 21 and features shown in, for example, Fig. 8. No new matter has been added.

Claim Rejections Under 35 U.S.C. § 102(e)

The Applicant believes the amendments presented herein overcome all rejections since the cited references do not teach all the claim limitations, either explicitly or impliedly. Specifically, claim 20 includes "a gate, common to both said n-channel field effect transistor and said p-channel field effect transistor, wherein said gate is formed in a layer of polysilicon; and a connection between a drain of the p-channel field effect transistor and a drain of the n-channel field effect transistor formed in said same layer of polysilicon, wherein the polysilicon comprising said gate is coplanar with the polysilicon comprising said connection between said drain of the p-channel field effect transistor and said drain of the n-channel field effect transistor." Neither Asami nor Wei teaches these limitations.

The gates 202, 302 of the NMOS and PMOS transistors 112 and 114 are not common. Hence, Wei does not teach the Applicant's claimed invention.

Likewise, Asami does not teach the Applicant's claimed invention. The polysilicon layer 52 of Asami forms the gate region of a subsequent transistor pair (Fig. 6), not "a connection between a drain of the p-channel field effect transistor and a drain of the n-channel field effect transistor." In fact, nowhere does Asami teach that the layer 52 touches either drain 22 or drain 24. Hence, Asami does not teach the Applicant's claimed invention.

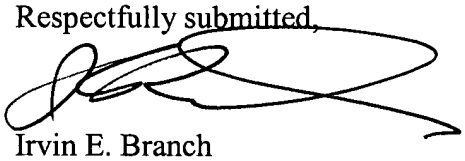
The remaining claims depend from claim 20 and are believed to be allowable, at least for the reasons stated above.

Conclusion

In view of the foregoing, the Applicant believes all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,



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Irvin E. Branch
Reg. No. 42,358

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, CA 94111-3834
Tel: 303-571-4000
Fax: 415-576-0300
IEB/jln
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